In the Specification

Please replace the paragraphs beginning on page 9, line19 and 22 with the following amended paragraphs:

FIG. 7 is a schematic of a current feedback amplifier equivalent in accordance with the present invention; ~~and~~

FIG. 8 is a schematic of a switched current feedback amplifier equivalent in accordance with the present invention[[.]]; and

FIG. 9 is a block diagram of a fast ethernet and ethernet driver in accordance with another embodiment of the present invention.

Please replace the paragraph beginning on page 10, line 4 with the following amended paragraph:

FIG. 5 shows a Fast Ethernet and Ethernet driver according to the present invention. The driver allows both a voltage source drive 51 to be used for Fast Ethernet and a bridge current source drive 52 to be used for Ethernet. The driver architecture uses 4 pins[[,]]; current source pins txp[[,]] and txn, and voltage source pins vp and vn. The expressions txp and txn are conventional terms for transmit positive and transmit negative respectively, while the expressions vp and vn indicate positive and negative termination voltages, respectively.

Please replace the paragraph beginning on page 10, line 14 with the following amended paragraph:

Line termination resistors 53, 54 connect to the two voltage ~~sources,~~source pins vp and vn. The two modes are combined by examining the termination resistors 53, 54, and by having two inputs. By reconfiguring the termination resistors it is possible to implement either of the two modes. The choice of which mode is ~~utilised~~utilized is made using standard techniques such as those described previously.

Please replace the paragraph beginning on page 10, line 22 with the following amended paragraph:

In the case of Fast Ethernet, the bridge currents, (I1, I2, I3 and I4) are turned off, as will be described in greater detail subsequently with reference to FIG. 8, and the line is voltage driven from vp and vn. As Fast Ethernet is required, the txp, txn signal drive level is 0.5V to -0.5V.

Please replace the paragraph beginning on page 10, line 28 with the following amended paragraph:

The line termination resistor r1 (53) is effectively in series with r3 and r2 (54) is in series with r4 for an incremental signal analysis. In order to obtain the required txp, txn signal, it is necessary to supply +1V, -1V at vp, vn. The load current is thus [[Vp]]vp/ (r1+r3) or 1V/(100 Ohms); that is, 10mA. The presented voltage at vp, vn is such that a differential of 2V exists. As such, the on chip voltage drop is 3.3V - 2V or 1.3V. This results in an on-chip power dissipation of 1.3V*10mA, which is equal to 13mW.

Please replace the paragraph beginning on page 12, line 4 with the following amended paragraph:

A more detailed representation of an implementation for ~~cable driver for~~ the Fast Ethernet and Ethernet Driver of FIG. 5 is shown in the schematic of FIG. 6A. The cable driver includes two current feedback amplifiers with a gain of -2. In Fast Ethernet mode, the logic

input, Enable, turns off the Ethernet, or 10BaseT, output currents. The amplifier pamp2 controls the output voltages, vp and vn, and V(vp, vn) = V(txp,txn)*2.

Please replace the paragraph beginning on page 12, line 11 with the following amended paragraph:

The drivers in accordance with the present invention ~~utilise~~utilize a new method to generate the bridge currents. In FIG. 6A, the 10BaseT current supplied to the line is from the outputs, Ioutp and Ioutn, of the amplifier pamp4, (see FIG. 8 for details). The currents Ioutp and Ioutn are ratios of the amplifier currents flowing in r3 and r4. In the case of pamp4, mp2 is 10 times the size of mp20, so the current in mp20 is 10 times the current in mp2. Ethernet driver circuits are conventionally biased from a fixed bandgap voltage, Vref, and an external resistor, Rext.

Please replace the paragraph beginning on page 13, line 11 with the following amended paragraph:

FIG. 7 is an equivalent circuit of the differential current feedback amplifier, pamp2, of FIG. 6A. The amplifier signals are referenced to half the power supply voltage, Vmid = 1.65V. With two inputs and two outputs, the amplifier responds to the current input at inp and inn.

Please replace the paragraph beginning on page 13, line 24 with the following amended paragraph:

When the input, inp, is at the same voltage as the input, vmid, then no current flows in the input inp. When the voltage at input inp is below vmid, then there is a signal current flowing in mn1 in addition to the Imn9 current. This signal current is converted to a voltage gain at the gate of mp2. The current in mp2 increases, providing a current at outp flowing from vcc to outp.

Please replace the paragraph beginning on page 13, line 31 with the following amended paragraph:

Also, when the voltage at input inp is below vmid, then the current flowing in mp1 is the Imn9 current minus the signal current. This signal current is converted into a voltage gain at the gate of mn2. The current in mn2 decreases, providing less current flowing from outp to gnd.

Please replace the paragraph beginning on page 14, line 6 with the following amended paragraph:

The switched current feedback amplifier pamp4 of FIG. 6A (illustrated in FIG. 8) is similar to the FIG. 7 amplifier except for the addition of a logic control, Enable, and the current outputs Ioutn and Ioutp. The logic input, Enable, switches the output of the amplifier.

Please insert a new paragraph, after the paragraph below which begins on page 14, line 20:

When Enable is low, mp9, mp10, mn12, and mn13 turn on. This shuts off the output currents in mp2, mp20, mp4, mp40, mn2, mn20, mn4, and mn40. The currents in mp20, mp40, mn20 and mn40 are controlled by the current feedback amplifier pamp4. The Ethernet bridge currents, at mp2, mp4, mn2, and mn4, are a scaled version of the amplifier currents. In this particular implementation, the scaling factor is 10 times.

Another embodiment is shown in Fig. 9, wherein respective first and second logic control signals are input to each of the first and second driving means for enabling and disabling the respective first and second driving means. In this arrangement, when one of the first or second driving means is enabled, the other driving means is disabled.